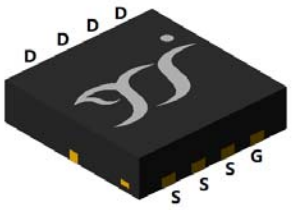
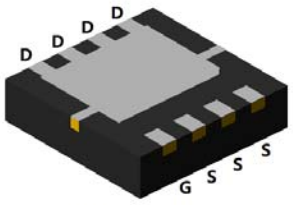
N-Channel Enhancement Mode Field Effect Transistor

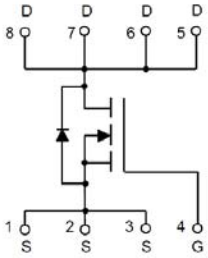


Top View



Bottom View

DFN3333-8L



Product Summary

- V_{DS} 40V
- I_D 35A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜8.0mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜13.0mΩ
- 100% EAS Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- 12V Automotive systems

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	12.5	A
	T_A =100℃		8	
	T_C=25℃		35	
	T_C =100℃		33	
Pulsed Drain Current [A]		I_{DM}	160	A
Avalanche energy [B]		EAS	144	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	2.2	W
	T_A =100℃		0.9	
	T_C=25℃		40	
	T_C =100℃		16	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	3.1	℃/W
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	55	℃/W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ35N04AQ	F1	Q35N04	5000	10000	100000	13" reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	5.5	8.0	mΩ
		V_{GS}=4.5V, I_D=10A	-	7.5	13	
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	0.9	1.2	V
Gate resistance	R_G	f=1MHz	-	1.7	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1MHz	-	2020		pF
Output Capacitance	C_{oss}		-	220		
Reverse Transfer Capacitance	C_{rss}		-	175		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=20V, I_D=20A	-	46	-	nC
Gate-Source Charge	Q_{gs}		-	6	-	
Gate-Drain Charge	Q_{gd}		-	11	-	
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=300A/us	-	20	-	nC
Reverse Recovery Time	t_{rr}		-	21	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=20V,I_{DS}=20A	-	7	-	ns
Turn-on Rise Time	t_r		-	56	-	
Turn-off Delay Time	$t_{D(off)}$		-	39	-	
Turn-off fall Time	t_f		-	2.6	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. V_{DD}=38V, V_G=10V , L=1mH, IAS=17A.
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in the still air environment with T_A =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design..

■Typical Electrical and Thermal Characteristics Diagrams

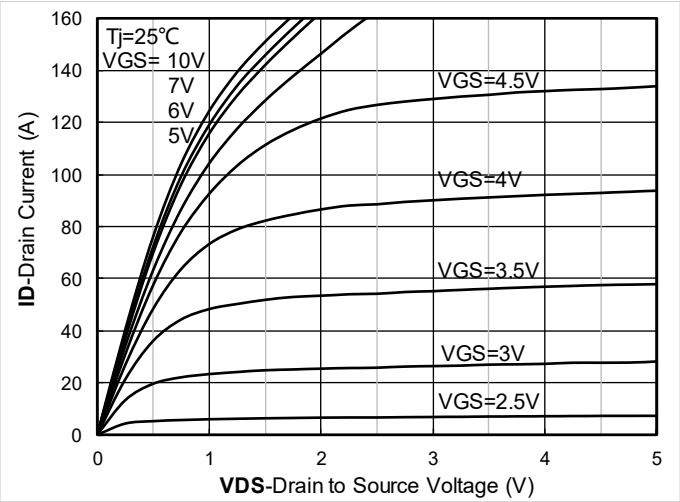


Figure 1. Output Characteristics

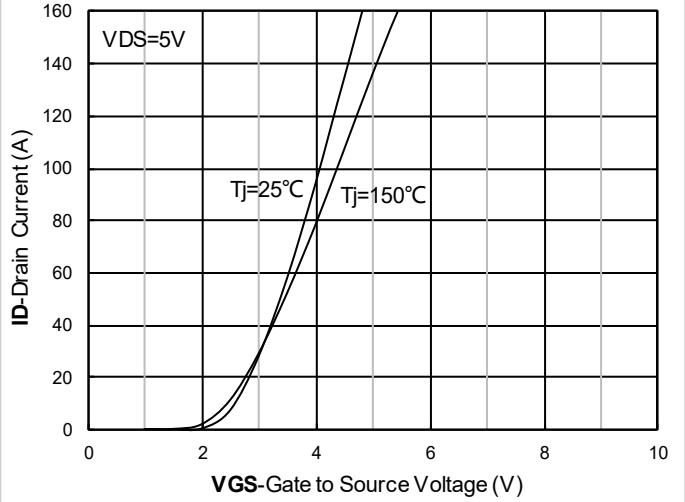


Figure 2. Transfer Characteristics

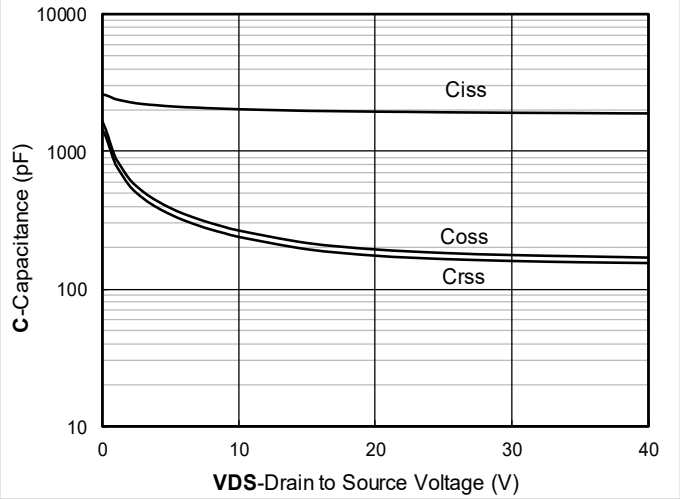


Figure 3. Capacitance Characteristics

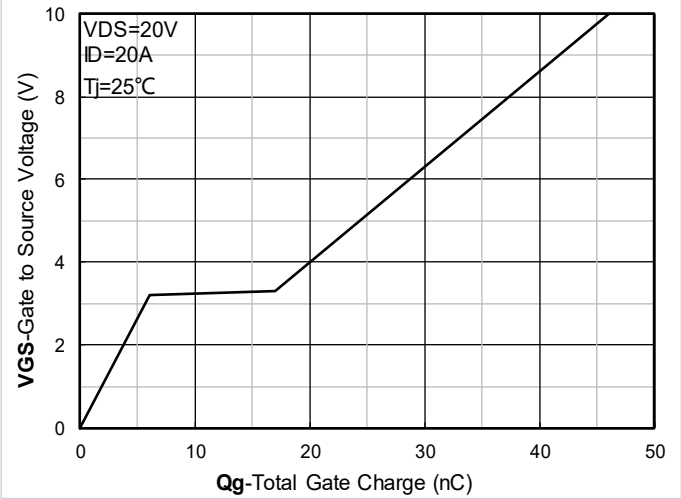


Figure 4. Gate Charge

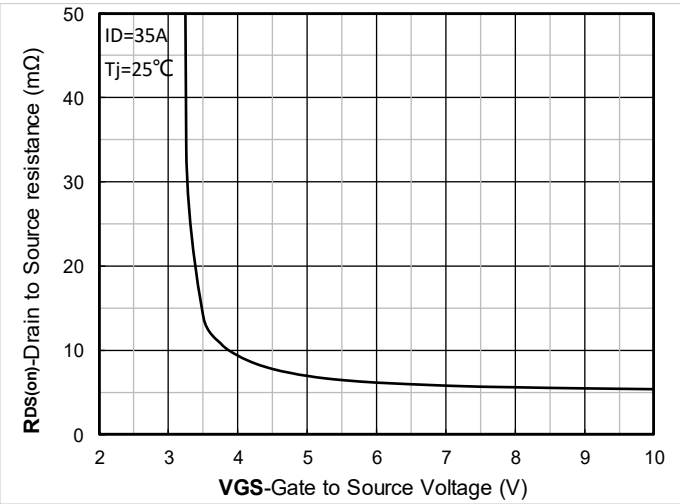


Figure 5. On-Resistance vs Gate to Source Voltage

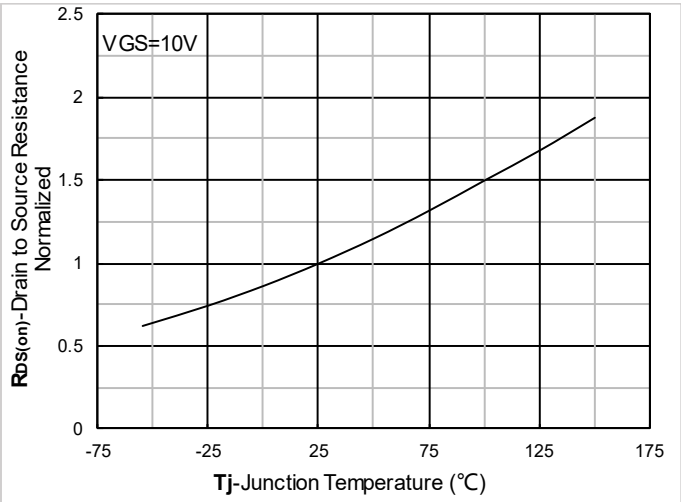


Figure 6. Normalized On-Resistance

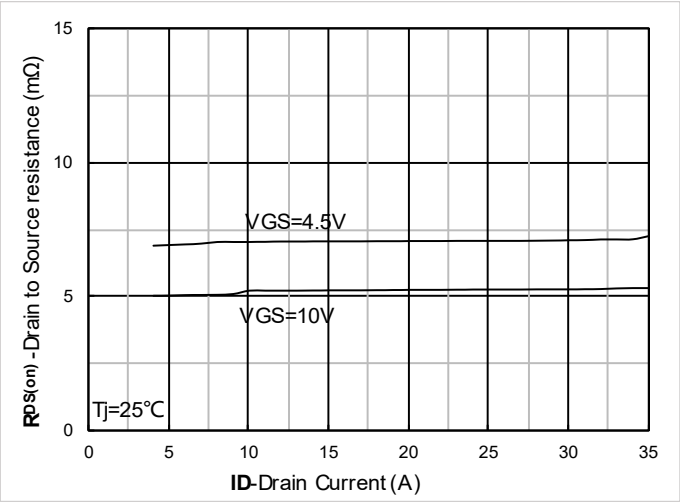


Figure 7. $R_{DS(on)}$ VS Drain Current

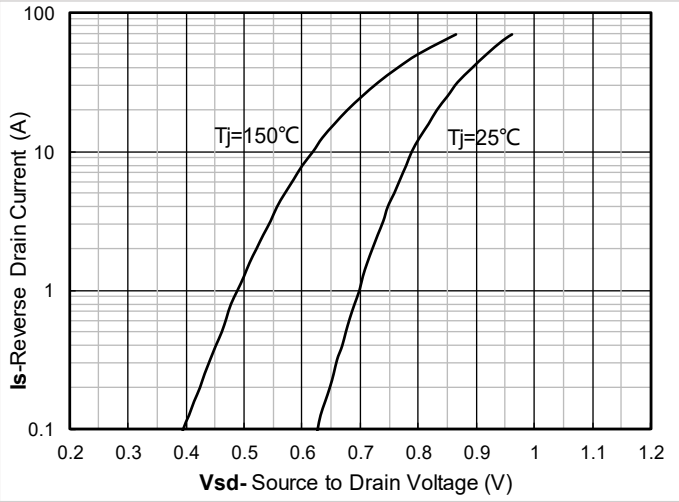


Figure 8. Forward characteristics of reverse diode

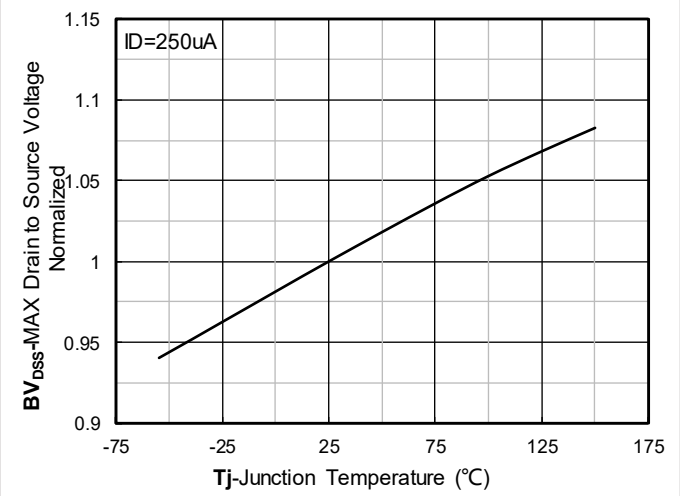


Figure 9. Normalized breakdown voltage

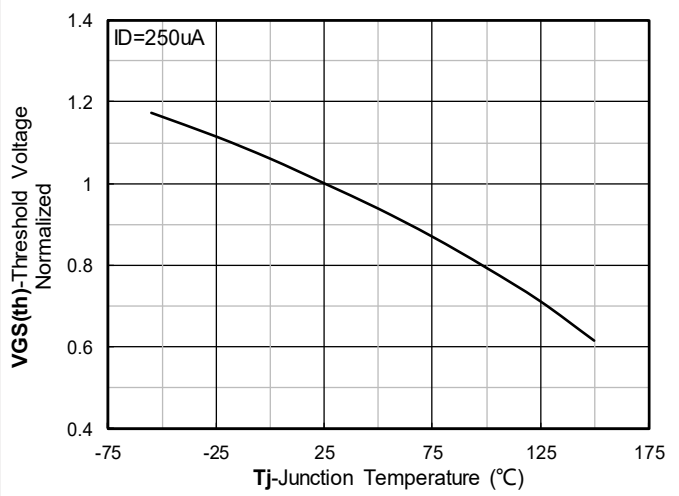


Figure 10. Normalized Threshold voltage

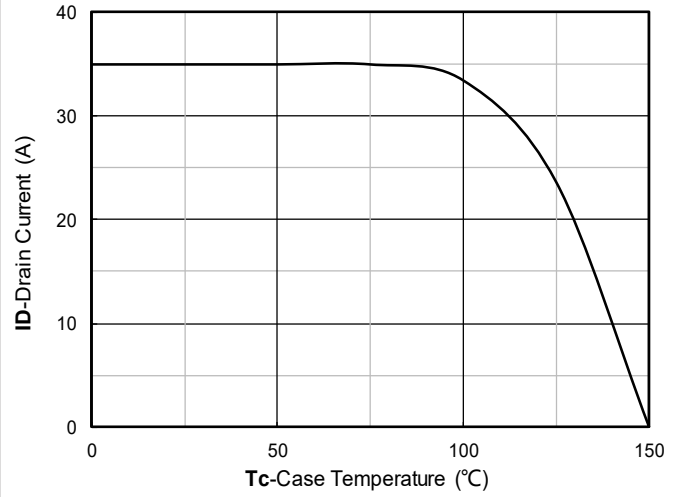


Figure 11. Current dissipation

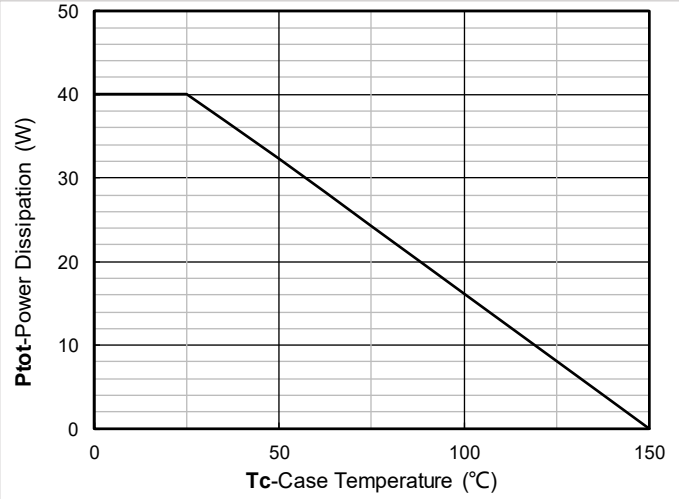


Figure 12. Power dissipation

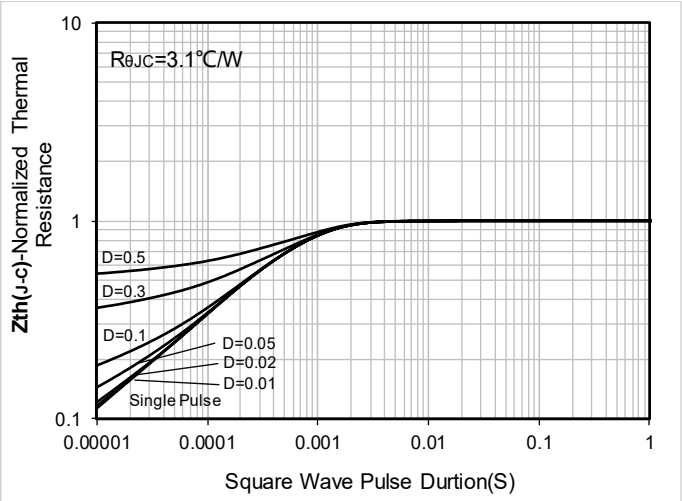


Figure 13. Maximum Transient Thermal Impedance

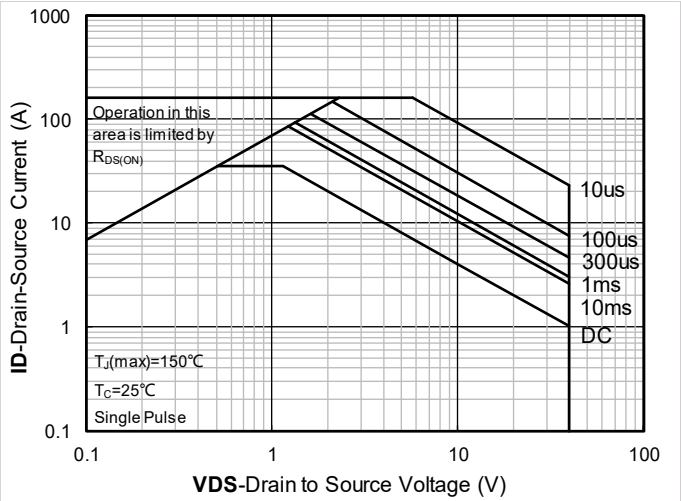
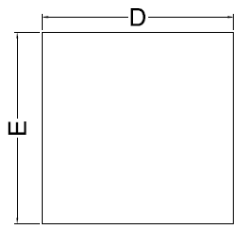
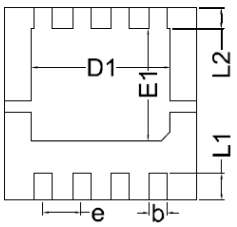


Figure 14. Safe Operation Area

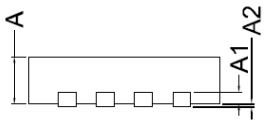
■DFN3333-8L Package information



Top View
正面视图

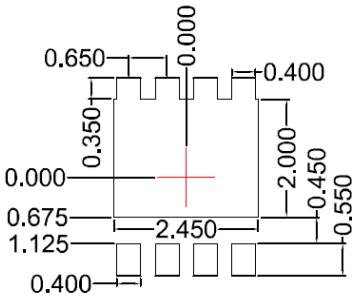


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2		0.35 BSC	
b	0.20	0.30	0.40
e		0.65 BSC	



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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